AMENDMENTS TO THE CLAIMS

(IN FORMAT COMPLIANT WITH THE REVISED 37 CFR 1.121)

1. (CURRENTLY AMENDED) A bus comprising:

a master interface connectable to a master device external to said bus and configured to (i) receive an early command signal ~~having a predetermined timing relationship to~~ from said master device a first clock edge of a system clock and (ii) present a bus wait signal to said master device proximate a second clock edge of said system clock;

a slave interface connectable to a slave device external to said bus and configured to (i) present a command signal to said slave device a delay after said first clock edge and (ii) receive a slave wait signal from said slave device; and

a control logic configured to (i) register said early command signal with said system clock to generate said command signal and (ii) convert said slave wait signal into said bus wait signal.

2. (CURRENTLY AMENDED) The bus according to claim 1, wherein (i) said master interface is further configured to receive an early address signal ~~having said predetermined timing relationship with~~ from said master device before said first clock edge, (ii) said control logic is further configured to register

said early address signal with said system clock to generate an address signal and decode said address signal to generate a device select signal, and (iii) said slave interface is further configured to present said address signal and said device select signal to said slave device said delay after said first clock edge.

3. (CURRENTLY AMENDED) The bus according to claim 2, wherein (i) said master interface is further configured to receive a no-address signal ~~having said predetermined timing relationship to~~ from said master device before said first clock edge and (ii) said control logic is further configured to inhibit said device select signal in response to said no-address signal.

4. (CURRENTLY AMENDED) The bus according to claim 1, wherein (i) said master interface is further configured to receive an early burst request signal ~~having said predetermined timing relationship to~~ from said master device before said first clock edge, (ii) said control logic is further configured to register said early burst request signal with said system clock to generate a burst request signal, and (iii) said slave interface is further configured to present said burst request signal to said slave device said delay after said first clock edge.

5. (CURRENTLY AMENDED) The bus according to claim 1, wherein (i) said master interface is further configured to receive a bus request signal from said master device and present a bus grant signal to said master device, and (ii) said control logic is further configured to arbitrate in response to said bus request signal and generate said bus grant signal.

6. (CURRENTLY AMENDED) The bus according to claim 5, wherein said control logic is further configured to complete arbitration within one clock cycle of said system clock and present said command signal in a next clock cycle of said system clock.

7. (CURRENTLY AMENDED) The bus according to claim 5, wherein (i) said master interface is further configured to receive a lock signal from said master device, and (ii) said control logic is further configured to halt arbitration responsive to said lock signal.

8. (ORIGINAL) The bus according to claim 1, wherein said control logic comprises an address decoder configured to generate a plurality of device select signals responsive to an address signal.

9. (CURRENTLY AMENDED) The bus according to claim 8, wherein said control logic further comprises a plurality of registers configured to register a plurality of early signals with said system clock, each of said early signals being valid before ~~having said predetermined timing relationship to~~ said first clock edge to generate a plurality of signals said delay after said first clock edge.

10. (ORIGINAL) The bus according to claim 9, wherein said control logic further comprises an arbitration logic configured to generate a bus grant signal.

11. (CURRENTLY AMENDED) The bus according to claim 10, wherein said control logic further comprises a first multiplexer configured to multiplex said early signals from said master interface to said slave interface responsive to said bus grant signal.

12. (CURRENTLY AMENDED) The bus according to claim 11, wherein said control logic further comprises a second multiplexer configured to ~~select a write data select signal~~ multiplex a plurality of write data select signals from said master interface to said slave interface responsive to said bus grant signal.

13. (CURRENTLY AMENDED) A method for operating a bus connectable to a master device and a slave device both external to said bus, comprising the steps of:

(A) receiving an early command signal ~~having a predetermined timing relationship to~~ before a first clock edge of a system clock at a master interface of said bus from said master device;

(B) registering said early command signal with said system clock to generate a command signal;

(C) presenting said command signal a delay after said first clock edge at a slave interface of said bus to said slave device;

(D) receiving a slave wait signal at said slave interface from said slave device;

(E) converting said slave wait signal into a bus wait signal; and

(F) presenting said bus wait signal at said master interface to said master device proximate a second clock edge of said system clock.

14. (CURRENTLY AMENDED) The method according to claim 13, further comprising the steps of:

receiving an early address signal ~~having said predetermined timing relationship with~~ before said first clock edge at said master interface from said master device;

registering said early address signal in response to said first clock edge to generate an address signal;

presenting said address signal at said slave interface to said slave device said delay after said first clock edge;

decoding said address signal to generate a device select signal in response to generating said address signal; and

presenting said device select signal at said slave interface to said slave device in response to decoding said address signal.

15. (CURRENTLY AMENDED) The method according to claim 14, further comprising the steps of:

receiving a no-address signal ~~having said predetermined timing relationship to~~ before said first clock edge at said master interface from said master device; and

inhibiting said device select signal in response to receiving said no-address signal.

16. (CURRENTLY AMENDED) The method according to claim 13, further comprising the steps of:

receiving an early burst request signal ~~having said predetermined timing relationship to~~ before said first clock edge at said master interface from said master device;

registering said early burst request signal with said system clock to generate a burst request signal in response to said first clock edge; and

presenting said burst request signal at said slave interface to said slave device said delay after said first clock edge.

17. (CURRENTLY AMENDED) The method according to claim 13, further comprising the steps of:

receiving a bus request signal at said master interface from said master device;

arbitrating in response to receiving said bus request signal; and

generating a bus grant signal at said master interface to said master device in response to arbitrating.

18. (CURRENTLY AMENDED) The method according to claim 17, wherein arbitrating is completed within one clock cycle of said system clock and said command signal is presented in a next clock cycle of said system clock.

19. (CURRENTLY AMENDED) The method according to claim 17, further comprising the steps of:

receiving a lock signal at said master interface from said master device after ~~in response to generating said bus grant signal~~; and

halting arbitration in response to receiving said lock signal.

20. (CURRENTLY AMENDED) A bus connectable to a master device and a slave device both external to said bus, comprising:

means for receiving an early command signal ~~having a predetermined timing relationship to~~ before a first clock edge of a system clock at a master interface from said master device;

means for registering said early command signal with said system clock to generate a command signal;

means for presenting said command signal a delay after said first clock edge at a slave interface to said slave device;

means for receiving a slave wait signal at said slave interface from said slave device;

means for converting said slave wait signal into a bus wait signal; and

means for presenting said bus wait signal at said master interface to said master device proximate a second clock edge of said system clock.